REMARKS

By this Amendment, claims 1-12 are amended, and claim 13 is added. Thus, claims 1-13 are active in the application. Reexamination and reconsideration of the application are respectfully requested.

The specification and abstract have been carefully reviewed and revised in order to correct grammatical and idiomatic errors in order to aid the Examiner in further consideration of the application. The amendments to the specification and abstract are incorporated in the attached substitute specification and abstract. No new matter has been added.

Also attached hereto is a marked-up version of the substitute specification and abstract illustrating the changes made to the original specification and abstract.

In item 2 on page 2 of the Office Action, the Examiner objected to the specification for lacking a brief description of features which are illustrated in Figure 17. The Applicants respectfully disagree that the specification does not describe the features which are illustrated in Figure 17. The conventional synchronization circuit illustrated in Figure 17 is clearly disclosed in the Background of the Invention section of the specification (pages 1-3 of the original and substitute specifications). Accordingly, the Applicants respectfully request the Examiner to withdraw the objection to the specification.

The Applicants thank the Examiner for kindly indicating, in item 5 on page 3 of the Office Action, that claims 2-5 and 7-8 are allowed. Although the Examiner did not address claims 10-12, which were added in the September 26, 2003 Preliminary Amendment, the Applicants respectfully submit that claims 10-12 are also allowable since claims 10-12 depend from allowed claims 2-4, respectively.

Minor editorial revisions were made to claims 2-5, 7-8 and 10-12 in order to improve their U.S. form. The Applicants submit that the revisions to claims 2-5, 7-8 and 10-12 were not to broaden or narrow their scope of protection for the present invention. Therefore, the Applicants respectfully submit that claims 2-5, 7-8 and 10-12, as amended, are still clearly in condition for allowance.

In item 4 on pages 2-3 of the Office Action, claims 1, 6 and 9 were rejected under 35 U.S.C. § 102(b) as being unpatentable over the Applicants' admitted prior art

(AAPA), as disclosed in Figure 17 and as described on pages 1-3 of the original and substitute specifications.

Without intending to acquiesce to the rejection of these claims, independent claim 1 has been amended in order to more clearly illustrate the marked differences between the present invention and the AAPA. Accordingly, the Applicants respectfully submit that claims 1, as well as claims 6, 9 and 13 which depend therefrom, are clearly allowable over the AAPA for the following reasons.

The present invention and the AAPA both provide a synchronization circuit which seeks to solve the problem of accurately latching data with a clock when there is a clock edge that is synchronized with an indefinite period (such as the period of Td shown in Figure 1 of the present invention, for example) which is located at a transition point of the inputted data by delaying the data so as to enable the data to be latched by the clock.

The present invention, as recited in claim 1, provides a synchronization circuit for receiving an input signal and a clock having a frequency which is equal to a transfer rate of the input signal, and for synchronizing the input signal with the clock. The synchronization circuit of claim 1 comprises a state detection circuit for receiving the input signal and the clock, and outputting a control signal according to the temporal relationship between a transition point of the input signal and an edge of the clock. The synchronization circuit of claim 1 also comprises a delay selection circuit for receiving the input signal and the control signal outputted from the state detection circuit, adding a delay to the input signal on the basis of the control signal, and outputting an output signal. The synchronization circuit of claim 1 also comprises a latch circuit for receiving the clock and the output signal outputted from the delay selection circuit, synchronizing the output signal outputted from the delay selection circuit with the clock and outputting the synchronized signal.

The AAPA discloses a synchronization circuit which includes a first latch circuit (flip flop) 1 and a second latch circuit 2 which each receive the input signal SIN. The second latch circuit 2 receives the clock SCK, whereas the first latch circuit 1 receives the inverted clock nSCK (clock SCK out of phase by 180 degrees) from the inverter 5. As described beginning at line 14 on page 1 of the original specification (line 15 on page 1 of the substitute specification), the first latch circuit 1 latches the input signal SIN at a

timing of a rising edge of the inverse clock nSCK. The second latch circuit 2 latches the input signal SIN at a timing of a rising edge of the clock SCK.

The AAPA also includes a selection circuit 4 which selects one of the latched (delayed) outputs of the first or second latch circuit 1, 2 based on a control signal CTL which is outputted from a switching control circuit 6. Accordingly, the selection circuit 4 is controlled to select either the latched output of the first latch circuit 1 or the latched output of the second latch circuit 2 by the control signal CTL which is outputted from the switching control circuit 6. The switching control circuit 6 receives the clock, and outputs the control signal CTL according to the temporal relationship between a transition point of the input signal SIN and an edge of the clock SCK. In particular, the switching control circuit 6 monitors the temporal relationship between the transition point of the input signal SIN and the edge of the clock SCK, and outputs the control signal CTL when detecting that the temporal relationship approaches a predetermined period of time. A third latching circuit 3 receives the latched output signal which is selected by the selection circuit 4 and synchronizes the selected signal with the clock SCK.

However, the signal which is latched at the inverse clock nSCK has already been output from the selection circuit 4 when the switching control circuit 6 detects that the transition point of the input signal SIN approaches the edge of the synchronous clock SCK, and this signal is again latched at the clock SCK by the third latch circuit 3, and therefore, a latency is undesirably added to the signal.

In contrast to the AAPA, the delay selection circuit of claim 1 receives the input signal and the control signal outputted from the state detection circuit, and adds a delay to the input signal on the basis of the control signal.

The Examiner has asserted that the selection circuit 4 of the AAPA corresponds to the delay selection circuit of claim 1. However, the selection circuit 4 of the AAPA does not, by itself, delay the input signal SIN. Instead, the input signal SIN is delayed by the first and second latch circuits 1, 2 by being latched at the inverse clock nSCK and the clock SCK, respectively, and the selection circuit 4 merely selects one of the latched outputs of the first and second latch circuits 1, 2 according to the control signal CT which is outputted from the switching control circuit 6. Accordingly, the selection circuit 4, by itself, clearly does not delay the input signal on the basis of the control signal CTL since

the selection circuit merely selects either the latched output of the first latch circuit 1 or the latched output of the latch circuit 2.

Moreover, even if the first and second latch circuits 1, 2 and the selection circuit 4 are combined to correspond to the delay selection circuit of claim 1, such a combined circuit does not disclose or suggest the delay selection circuit of claim 1. As a collective circuit, the first and second latch circuits 1, 2, which delay the input signal at the inverse clock nSCK and the clock nSCK, respectively, and the selection circuit 4 receive the clock SCK or the inverse clock nSCK in addition to the input signal and the control signal CTL. The first and second latch circuits 1, 2 of the AAPA latch the input signals based on the clock SCK or the inverse clock nSCK, not the control signal CTL. As described above, the control signal CTL is merely used to control the selection circuit to select either the latched output of the first latch circuit 1 or the latched output of the second latch circuit 2. Therefore, the first and second latch circuits 1, 2 and the selection circuit 4 of the AAPA, as a collective circuit, delay the input signal by either the inverse clock nSCK or the clock SCK, not on the basis of the control signal.

Accordingly, the AAPA clearly does not disclose or suggest a delay selection circuit for receiving the input signal and the control signal outputted from the state detection circuit, adding a delay to the input signal on the basis of the control signal, and outputting an output signal, as recited in claim 1.

Therefore, the AAPA clearly does not disclose or suggest each and every limitation of claim 1. Accordingly, the Applicants respectfully submit that claim 1 is clearly not anticipated by the AAPA since the AAPA fails to disclose each and every limitation of claim 1.

Claim 1 is clearly distinguishable over the AAPA for the reasons given above. New claim 13 also clearly distinguishes the present invention over the AAPA. Claim 13 recites that delay selection circuit is operable to add a delay the input signal on the basis of the control signal without using the clock. As described above, the selection circuit 4 of the AAPA merely selects either the latched output of the first latch circuit 1 or the latched output of the second latch circuit 2. Accordingly, the selection circuit 4 of the AAPA does not, by itself, delay the input signal on the basis of the control signal without using the clock, as recited in claim 13. Further, even if the first and second latch circuits

1, 2 and the selection circuit 4 of the AAPA are combined to correspond to the delay selection circuit of the present invention, the first and second latch circuits 1, 2 delay the input signal on the basis of the inverse clock nSCK or the clock SCK, not the control signal CTL. Accordingly, even if the first and second latch circuits 1, 2 and the selection circuit 4 of the AAPA are combined to correspond to the delay selection circuit of the present invention, such a combined circuit clearly does not add a delay to the input signal on the basis of the control signal without using the clock, as recited in new claim 13.

Therefore, claims 1 and 13 are both clearly not anticipated by the AAPA since the AAPA clearly does not disclose or suggest each and every limitation of claims 1 and 13.

Because of the clear distinctions discussed above, it is submitted that the teachings of the AAPA clearly do not meet each and every limitation of claim 1. Furthermore, it is submitted that the distinctions are such that a person having ordinary skill in the art at the time the invention was made would not have been motivated to modify the AAPA in such as manner as to result in, or otherwise render obvious, the present invention as recited in claim 1. Therefore, it is submitted that the claim 1, as well as claims 6, 9 and 13 which depend therefrom, are clearly allowable over the prior art as applied by the Examiner.

In view of the foregoing amendments and remarks, it is respectfully submitted that the present application is clearly in condition for allowance. An early notice thereof is respectfully solicited.

If, after reviewing this Amendment, the Examiner feels there are any issues remaining which must be resolved before the application can be passed to issue, the Examiner is respectfully requested to contact the undersigned by telephone in order to resolve such issues.

Respectfully submitted,

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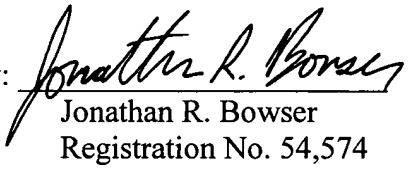
By: 

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